ITE 聯陽半導體 ITE Tech. Inc.

IT7230AFN / IT7230BFN / IT7231FN

Single Electrode Cap Sensor Controller

Preliminary Specification V0.4.3

(For B Version)

ITE TECH. INC.

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Additional copies of this manual or other ITE literature may be obtained from:

ITE Tech. Inc.
Marketing Department
7F, No.233-1, Baociao Rd., Sindian City,
Taipei County 23145, Taiwan, ROC

Tel: 886-2-29126889
Fax: 886-2-2910-2551, 886-2-2910-2552

If you have any marketing or sales questions, please contact:
P.Y. Chang, at ITE Taiwan:
E-mail: p.y.chang@ite.com.tw, Tel: 886-2-29126889 X6052, Fax: 886-2-29102551

You may also find the local sales representative nearest you on the ITE web site.

To find out more about ITE, visit our World Wide Web at:
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Or e-mail itesupport@ite.com.tw for more product information/services

Revision History

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12	Top Marking Information Added CODE NO. on the top marking.	29

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TABLES

1. Features

- **Programmable Capacitance-to-Digital Converter(CDC)**
  - Maximum 13 capacitance sensor inputs
  - 9 ms update rate, all 13 sensor inputs
  - No external RC components required
  - Automatic conversion sequencer
- **On-chip Automatic Calibration Logic**
  - Automatic calibration & compensation for environmental changes
  - Automatic adaptive threshold and sensitivity levels
- **On-chip RAM to Store Calibration Data**
  - Hardware initialization of SRAM
  - Host can access SRAM freely at any time
- **Supports 1 Interrupt Output and 2 Touch Detection Outputs**
- **Supports a Maximum of 13 General Purpose Input/Output (GPIO)**
- **Supports a Maximum of 15 Current-Control Output for LED Dimming Function**
- **Supports Dynamic Power Saving Mode**
  - Provides three operational modes: active, idle and sleep modes
  - Provides host special commands to switch between these modes
- **Hardware Slider Function**
  - Provides two 32-level hardware auto slider function
- **I^2C Compatible Interface (IT7230AFN/BFN)**
  - Compliant to I^2C specification v2.1
  - Supports slave device only
  - Supports standard and fast modes
  - 7-bit device addressing modes
  - Supports 2 address select pins to configure the device address selection (IT7230AFN only)
- **SPI Compatible Interface (IT7231FN)**
  - Compliant to 4-wire serial peripheral interface (SPI)
- **Operation Power**
  - One power source 2.5V ~ 3.6V
  - Provides one internal power regulator for core power generation
- **Low Power Consumption**
  - Active mode: 550 uA
  - Idle mode: 120 uA
  - Sleep mode: 30 uA
- **Package**
  - 40-pin QFN
  - 24-pin QFN
- **RoHS Compliant (100% Green Available)**

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2. General Description

The IT7230/7231 is one programmable controller with capacitance sensors which is used to implement functions such as buttons, scroll bars, and wheels. One single electrode capacitance-to-digital converter (CDC) is integrated into this controller.

The IT7230/7231 also provides a post-processing with CDC, and it can automatically calibrate and compensate the front-end CDC values for environmental changes. It also modifies the threshold and sensitivity levels automatically. The chip supports one interrupt output indicated that the CDC value over the user programming sensitivity level. It also supports two touch detection outputs indicated that the two corresponding sensor inputs over the default sensitivity level. The default sensitivity level can be automatically setting by the internal environment detection circuit without any software programming. So the user can use the two outputs to control the power-on or system reset function.

The IT7230/7231 supports one I^2C compatible interface to communicate with the host. It also supports two address select pins to specify the device ID addresses. Through this interface, the host can program the internal controlled registers to configure this chip to meet users' requirements. Furthermore, GPIO and current-control functions are supported to indicate the specific status or LED dimming by the user's definition.

The IT7230/7231 is available in 40-pad, 5 mm x 5 mm QFN package type and 24-pad, 4 mm x 4 mm QFN package type. And it operates with only one 2.5V~3.6V power supply.

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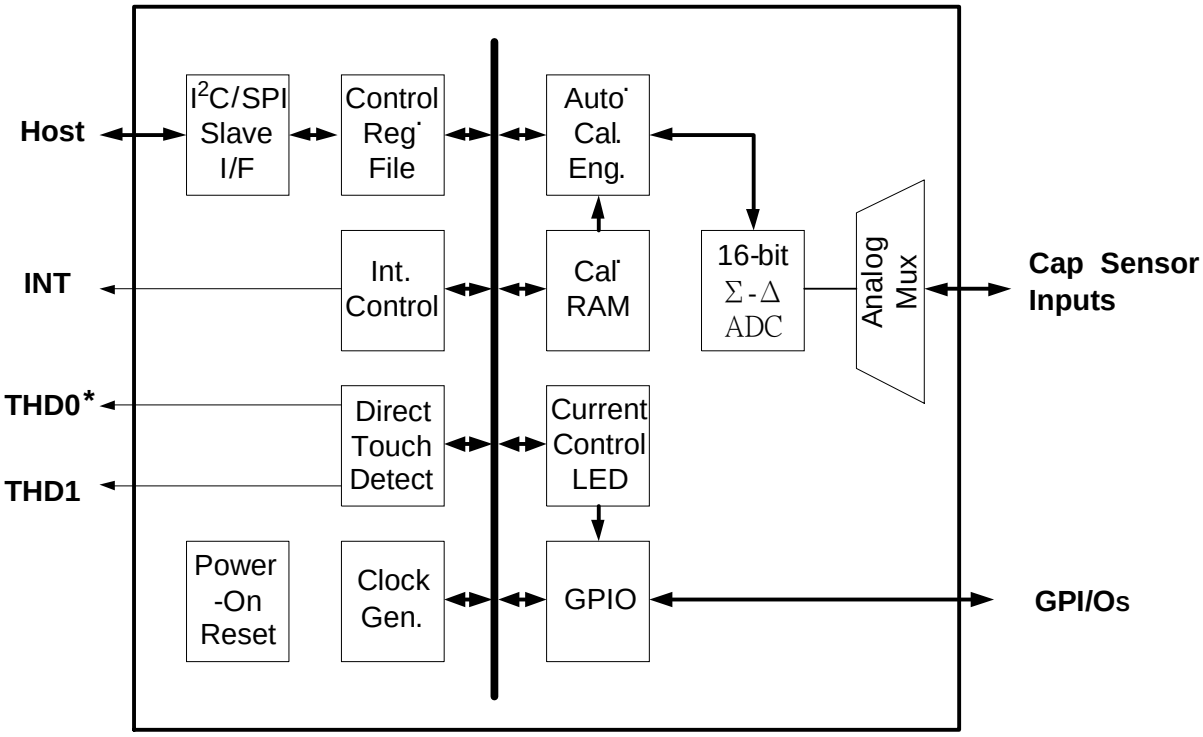
3. Block Diagram



* IT7230AFN/IT7231FN only

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4. Pin Configuration

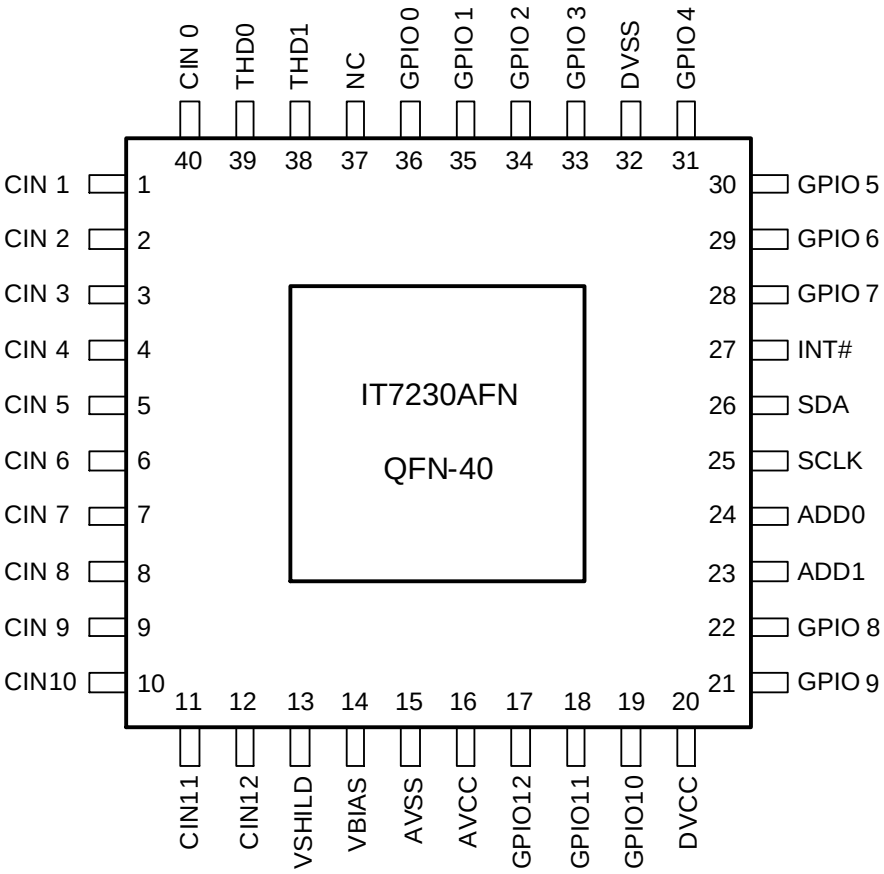

Table 4-1. IT7230AFN Pins Listed in Numeric Order (40-pin QFN)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	CIN1	11	CIN11	21	GPIO9	31	GPIO4
2	CIN2	12	CIN12	22	GPIO8	32	DVSS
3	CIN3	13	VSHILD	23	ADD1	33	GPIO3
4	CIN4	14	VBIAS	24	ADD0	34	GPIO2
5	CIN5	15	AVSS	25	SCLK	35	GPIO1
6	CIN6	16	AVCC	26	SDA	36	GPIO0
7	CIN7	17	GPIO12	27	INT#	37	NC
8	CIN8	18	GPIO11	28	GPIO7	38	THD1
9	CIN9	19	GPIO10	29	GPIO6	39	THD0
10	CIN10	20	DVCC	30	GPIO5	40	CIN0

Table 4-2. IT7230AFN Pins Listed in Alphabetical Order (40-pin QFN)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
ADD0	24	CIN6	6	GPIO1	35	GPIO11	18
ADD1	23	CIN7	7	GPIO2	34	GPIO12	17
AVCC	16	CIN8	8	GPIO3	33	INT#	27
AVSS	15	CIN9	9	GPIO4	31	NC	37
CIN0	40	CIN10	10	GPIO5	30	SCLK	25
CIN1	1	CIN11	11	GPIO6	29	SDA	26
CIN2	2	CIN12	12	GPIO7	28	THD0	39
CIN3	3	DVCC	20	GPIO8	22	THD1	38
CIN4	4	DVSS	32	GPIO9	21	VBIAS	14
CIN5	5	GPIO0	36	GPIO10	19	VSHILD	13

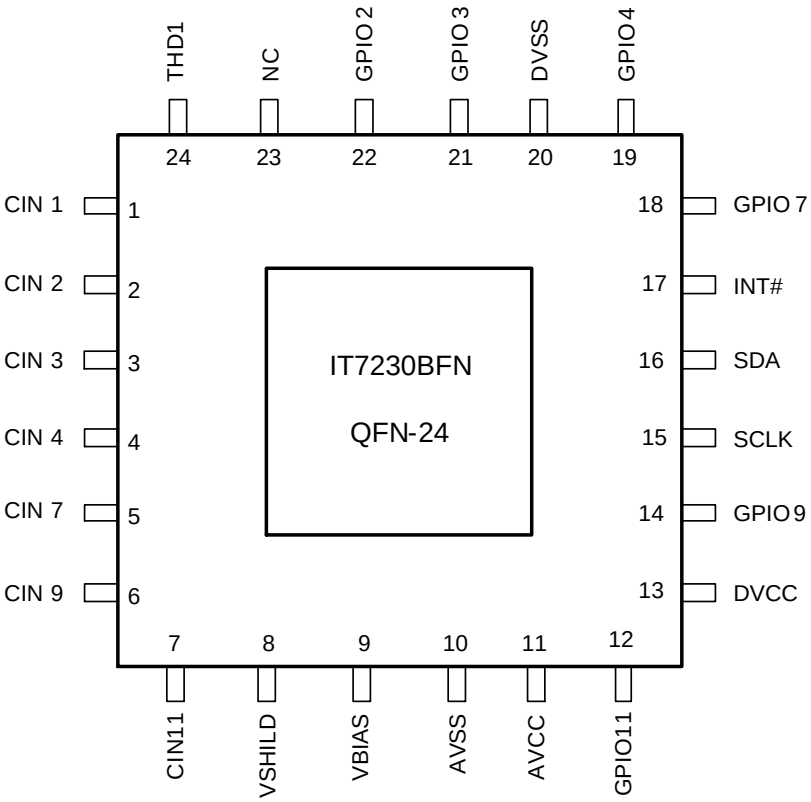

Table 4-3. IT7230BFN Pins Listed in Numeric Order (24-pin QFN)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	CIN1	7	CIN11	13	DVCC	19	GPIO4
2	CIN2	8	VSHILD	14	GPIO9	20	DVSS
3	CIN3	9	VBIAS	15	SCLK	21	GPIO3
4	CIN4	10	AVSS	16	SDA	22	GPIO2
5	CIN7	11	AVCC	17	INT#	23	NC
6	CIN9	12	GPIO11	18	GPIO7	24	THD1

Table 4-4. IT7230BFN Pins Listed in Alphabetical Order (24-pin QFN)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AVCC	11	CIN7	5	GPIO3	21	NC	23
AVSS	10	CIN9	6	GPIO4	19	SCLK	15
CIN1	1	CIN11	7	GPIO7	18	SDA	16
CIN2	2	DVCC	13	GPIO9	14	THD1	24
CIN3	3	DVSS	20	GPIO11	12	VBIAS	9
CIN4	4	GPIO2	22	INT#	17	VSHILD	8

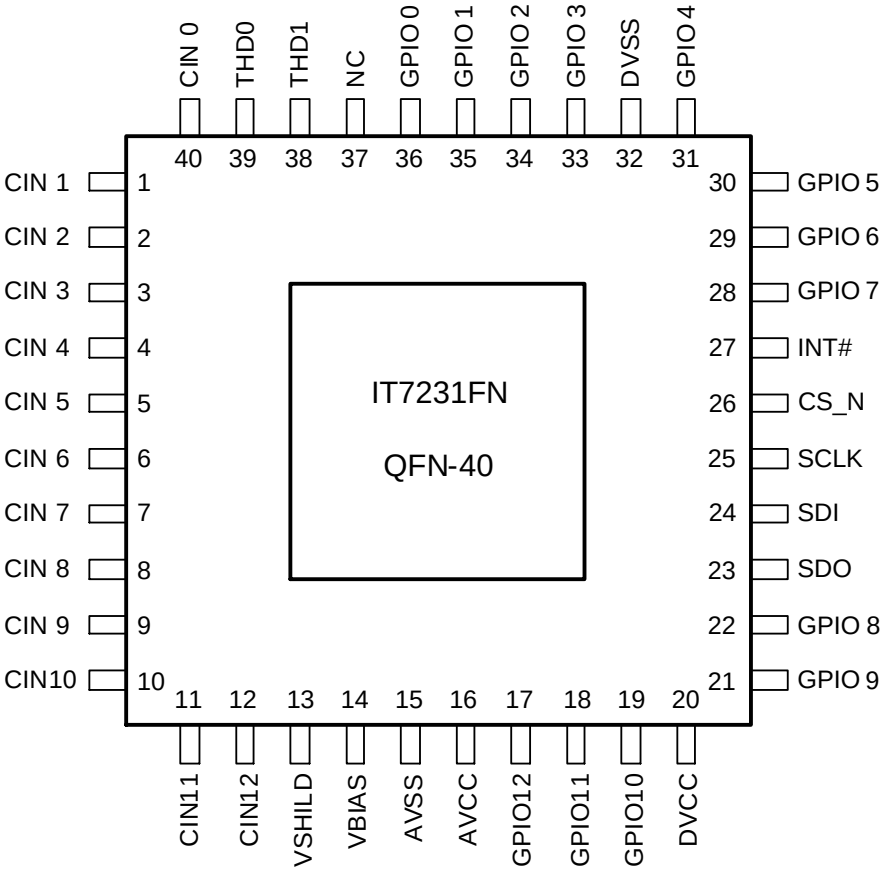

Table 4-5. IT7231FN Pins Listed in Numeric Order (40-pin QFN)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	CIN1	11	CIN11	21	GPIO9	31	GPIO4
2	CIN2	12	CIN12	22	GPIO8	32	DVSS
3	CIN3	13	VSHILD	23	SDO	33	GPIO3
4	CIN4	14	VBIAS	24	SDI	34	GPIO2
5	CIN5	15	AVSS	25	SCLK	35	GPIO1
6	CIN6	16	AVCC	26	CS_N	36	GPIO0
7	CIN7	17	GPIO12	27	INT#	37	NC
8	CIN8	18	GPIO11	28	GPIO7	38	THD1
9	CIN9	19	GPIO10	29	GPIO6	39	THD0
10	CIN10	20	DVCC	30	GPIO5	40	CIN0

Table 4-6. IT7231FN Pins Listed in Alphabetical Order (40-pin QFN)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AVCC	16	CIN8	8	GPIO2	34	GPIO12	17
AVSS	15	CIN9	9	GPIO3	33	INT#	27
CIN0	40	CIN10	10	GPIO4	31	NC	37
CIN1	1	CIN11	11	GPIO5	30	SCLK	25
CIN2	2	CIN12	12	GPIO6	29	SDI	24
CIN3	3	CS_N	26	GPIO7	28	SDO	23
CIN4	4	DVCC	20	GPIO8	22	THD0	39
CIN5	5	DVSS	32	GPIO9	21	THD1	38
CIN6	6	GPIO0	36	GPIO10	19	VBIAS	14
CIN7	7	GPIO1	35	GPIO11	18	VSHILD	13

5. Pin Description

Table 5-1. Pin Description of Capactiance Sensor Related Pins

Pin(s) No.		Signal		Attribute	Description
Capacitance Sensor Related Pins (Analog I/F)					
IT7230AFN /7231FN	**IT7230 BFN**	**IT7230AFN /7231FN**	**IT7230 BFN**		
40, 1-12	1-7	CIN0-12	CIN1-4 CIN7,9 CIN11	AI	***Capacitance Sensor Input Channels*** These inputs are used to sense the capacitance values. They can be companioned with capacitance sensors to implement functions such as buttons, scroll bars, and wheels.
14	9	VBIAS		AI	***Bias Voltage*** This pin must be connected to ground with one 0.1uF capacitor to supply one bias voltage.
13	8	VSHILD		AO	***CDC Active Shield Output*** This pin must be connected to the external plane.

Table 5-2. Pin Descriptions of General Purpose Input/Output

Pin(s) No.		Signal		Attribute	Description
General Purpose Input/Output (GPIO) (3.3V CMOS I/F, 5V tolerant)					
IT7230AFN /7231FN	**IT7230 BFN**	**IT7230AFN /7231FN**	**IT7230 BFN**		
36-33, 31-28, 22-21, 19-17	22-21, 19-18, 14,12	GPIO0-12	GPIO2-4 GPIO7 GPIO9 GPIO11	IOK16	***General Purpose Input/Output*** These pins can be used to indicate the corresponding functions of the capacitance sensors are active.

Table 5-3. Pin Descriptions of I^2C Interface (for IT7230AFN/IT7230BFN)

Pin(s) No.		Signal		Attribute	Description
I^2C Interface (3.3V CMOS I/F, 5V tolerant)					
IT7230AFN	**IT7230 BFN**	**IT7230AFN**	**IT7230 BFN**		
25	15	SCLK		IOK2	***I^2C Clock***
26	16	SDA		IOK2	***I^2C Data***
24-23	-	ADD1-0	-	IK	***I^2C Address Select Bit 1-0*** The bits are used to specify the decoded address of this chip.

Table 5-4. Pin Descriptions of SPI Interface (for IT7231FN)

Pin(s) No.	Signal	Attribute	Description
SPI Interface (3.3V CMOS I/F, 5V tolerant)			
25	SCLK	IK	***SPI Clock***
26	CS_N	IK	***SPI Chip Select***
23	SDO	O8	***SPI Output Data***
24	SDI	IK	***SPI Input Data***

Table 5-5. Pin Descriptions of Sensor Detected Pins

Pin(s) No.		Signal		Attribute	Description
Sensor Detected Pins (3.3V CMOS I/F)					
IT7230AFN /7231FN	**IT7230 BFN**	**IT7230AFN /7231FN**	**IT7230 BFN**		
27	17	INT#		O8	***General Interrupt Output*** When the CDC value is over the threshold value of the sensor input and the interrupt enable bit is active, the pin will change the state to low.
39-38	24	THD1-0	THD1	O8	***Touch Detection Output 1-0*** These pins are multi-function, and are selected by the configuration register. The default function of these pins is touch detection output. When the CDC value is over the default threshold value of the corresponding sensor input, the pin will change the state to high.

Table 5-6. Pin Descriptions of Power/Ground Signals

Pin(s) No.		Signal		Attribute	Description
Power Ground Signals					
IT7230AFN /7231FN	**IT7230 BFN**	**IT7230AFN /7231FN**	**IT7230 BFN**		
32	20	DVSS		I	***Digital Ground for Digital Component***
20	13	DVCC		I	***Digital VCC (3.3V) for Digital Component***
15	10	AVSS		I	***Analog Ground for Analog Component***
16	11	AVCC		I	***Analog VCC (3.3V) for Analog Component***
37	23	NC		IK	***Not Connected*** The pin can be floating.

Notes: I/O cell types are described below:

I: Input PAD.
AI: Analog Input PAD.
IK: Schmitt Trigger Input PAD.
AO: Analog Output PAD.
O8: 8 mA Output PAD.
IOK2: 2 mA Bidirectional PAD with Schmitt Trigger Input PAD.
IOK16: 16 mA Bidirectional PAD with Schmitt Trigger Input PAD.

6. Analog Performance

6.1 Test Conditions

The calibration engine registers set the calibration configuration.
AVCC = 3.3V
AVSS = 0V
Ta=25℃
Internal ADCCLK = 250Khz

Table 6-1. Analog Performance

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ADC					
Over-sampling Rate, OSR		64		256	clocks
Update-rate, Tperiod	OSR=64,128,256		13*64*3*(1/ADCCLK) 13*128*3*(1/ADCCLK) 13*256*3*(1/ADCCLK)		second
Output Noise, peak-to-peak	OSR=64,128,256			12,7,3	LSB
Resolution	No-missing code		16		bits
ADC Clock			250K		Hz
Capacitance					
Cstray, 7bits resolution	+/- 20%, note 1	0	-	20	PF
CIN 0-12, input range	+/- 20%, note 1			+/-8	PF
Power					
Full Power Mode	Full power mode	-	550	800	uA
Idle Mode	Note 2	-	120	150	uA
Sleep Mode	Note 3	-	30	40	uA

Notes:
1. Total unadjusted capacitance tolerance is +/- 20%.
2. LDO low power mode, power save timeout = 800ms, decimation rate = 64
3. PDCR = 0x000F.

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7. Serial Interface

7.1 Overview

The IT7230 is available with an I^2C –compatible interface. The IT7231 is available with an SPI-compatible interface. Both IT7230 and IT7231's serial interfaces support 4 transfer types - single write, burst write, single read, and burst read.

7.2 I^2C- Compatible Interface

The IT7230 supports 2-wire I^2C serial interface protocol of the industry standard. It is also compatible with System Management Bus(SMBus) protocol.

7.2.1 Device Address

IT7230 supports 4 different 7-bit device addresses which are controlled by the ADD0 and ADD1 pins. The related device addresses are listed below.

Table 7-1. IT7230 I^2C Device Address

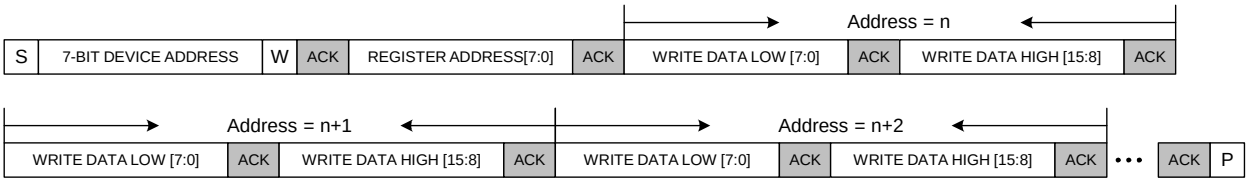
ADD1	ADD0	I^2C Address
0	0	1000 110
0	1	0110 101
1	0	1101 110
1	1	0010 111

7.2.2 Data Transfer

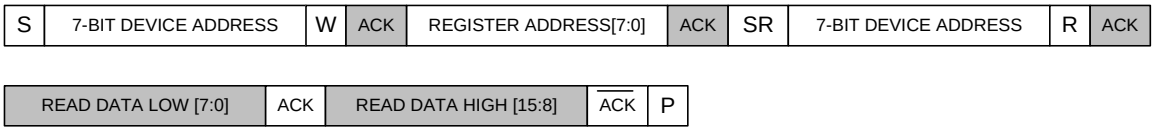
Data is transferred over the I^2C bus in 8-bit address and 16-bit data. IT7230 supports the following 4 transfer types. The related protocol and timing diagrams are shown below.

Single Write

Burst Write



Single Read



Burst Read

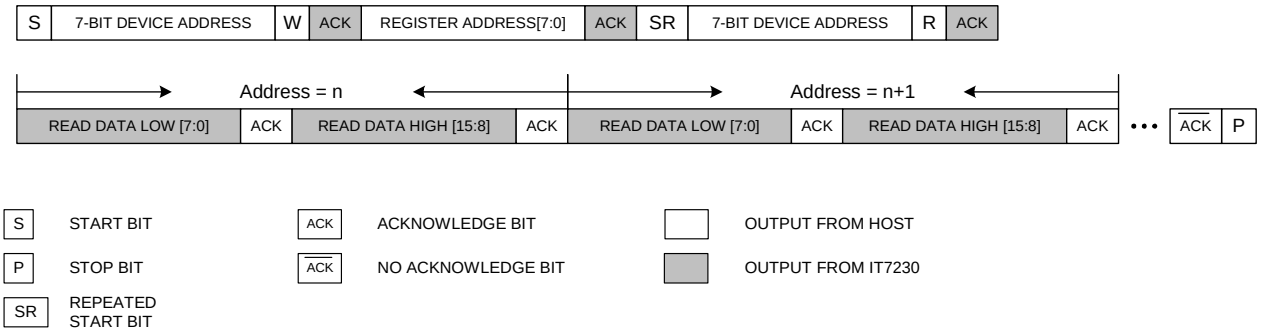


Figure 7-1. Example of I²C Timing for Single Register Write Operation

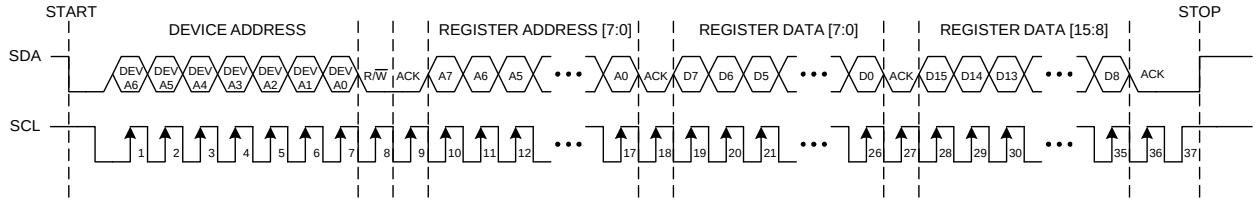
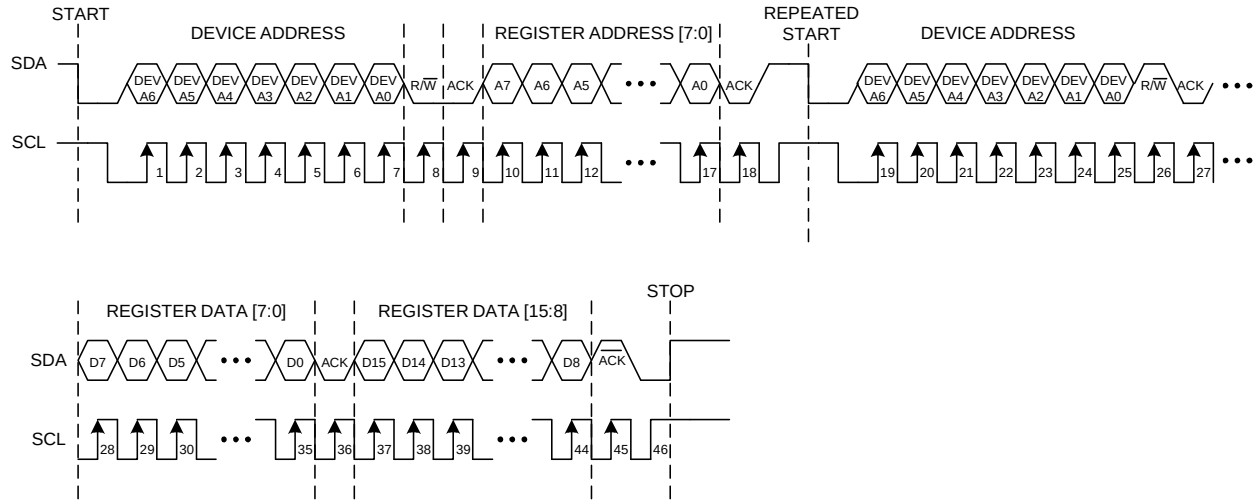


Figure 7-2. Example of I²C Timing for Single Register Read Operation



7.2.3 Timeouts

The IT7230 I²C interface supports a timeout reset mechanism to prevent I²C bus halt due to any abnormal transaction. If SCL is low over 4ms, the I²C interface will reset itself and be ready to receive a new command.

7.3 SPI- Compatible Interface

The IT7231 supports 4-wire serial peripheral interface (SPI) protocol of the industry standard. It has a data input pin (SDI) to input data from host to IT7231, a data output pin (SDO) to output data from IT7231 to host, and a clock input pin (SCLK) to support a reference clock for inputting and outputting data. A chip select (CS) is used to enable or disable the IT7231's serial interface. IT7231 supports both SPI mode 0 and mode 3.

7.3.1 Device Address

To start the transfer correctly, an appropriate 3-bit device address must be sent first. If users want to program on-chip OTP for initial parameter setting, the device address must be set to 3'b010. Otherwise, the registers of IT7231 should be distributed into 2 pages, page 0 and 1. To access registers of page 0, device address must be set to 3'b000 and 3'b001 is bound to page 1.

7.3.2 Data Transfer

After the device address, a 1-bit read/write direction bit is used to indicate the direction of the data transfer. This read/write bit is followed by 12-bit addresses necessary to be sent. But address bit [11:8] must be set to 4'b0000 and only bit [7:0] is useful for data transfer. If the value of read/write direction bit is 0(write), there should be 16-bit data sent from host after the address bits. On the contrary, if the read/write direction bit is 1(read), the read data is sent out from IT7231 through SDO pin.
The related protocol and timing diagrams are shown below.

Figure 7-3. Example of SPI Timing for Single Register Write Operation

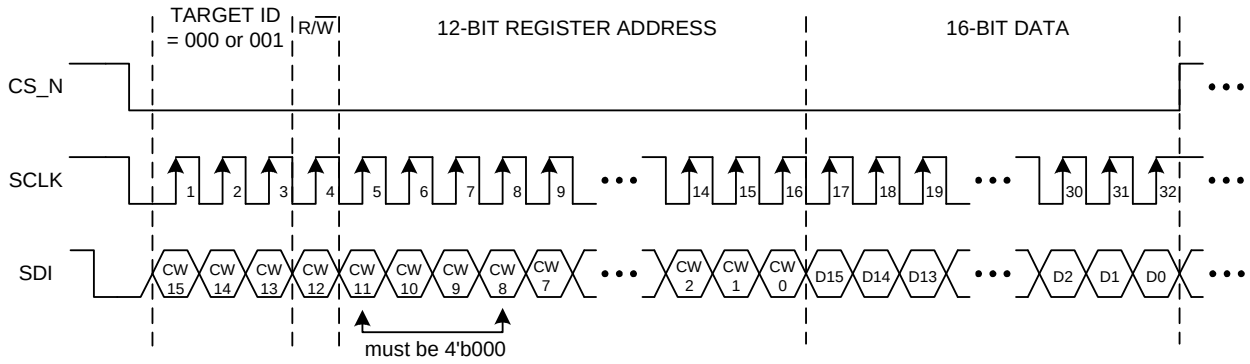


Figure 7-4. Example of SPI Timing for Burst Register Write Operation

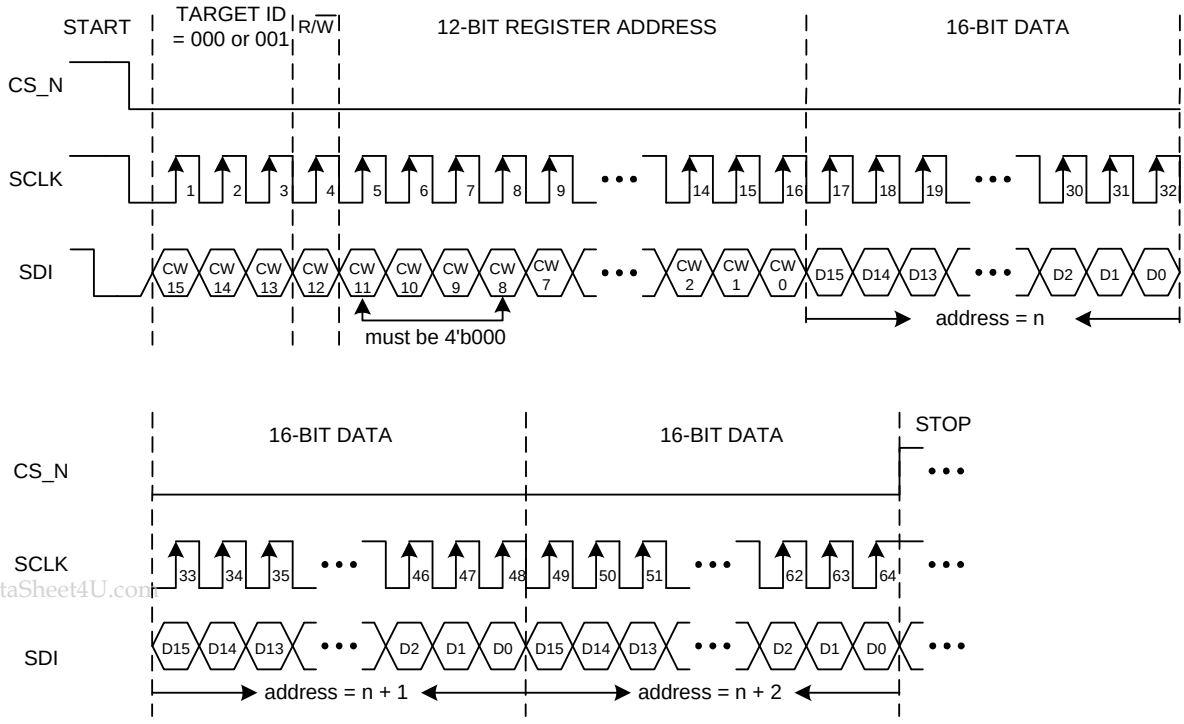


Figure 7-5. Example of SPI Timing for Single Register Read Operation

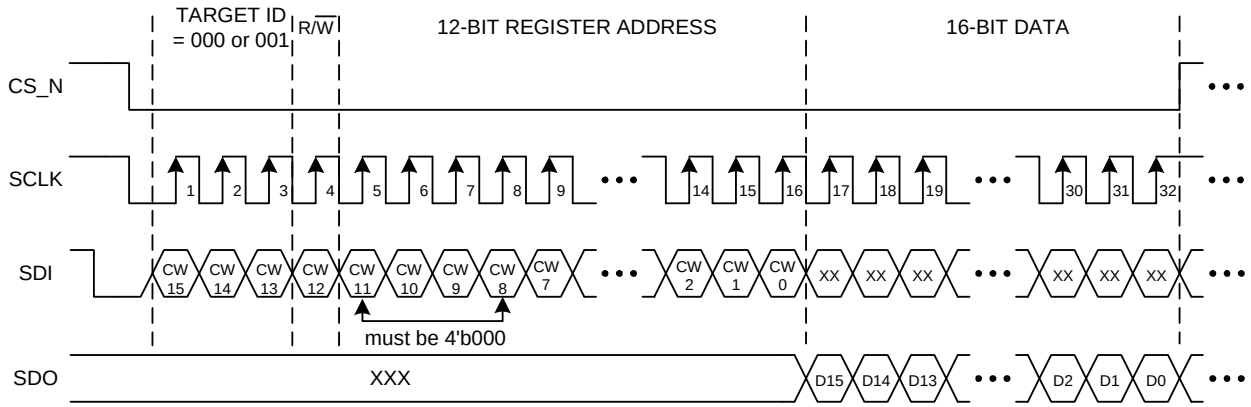
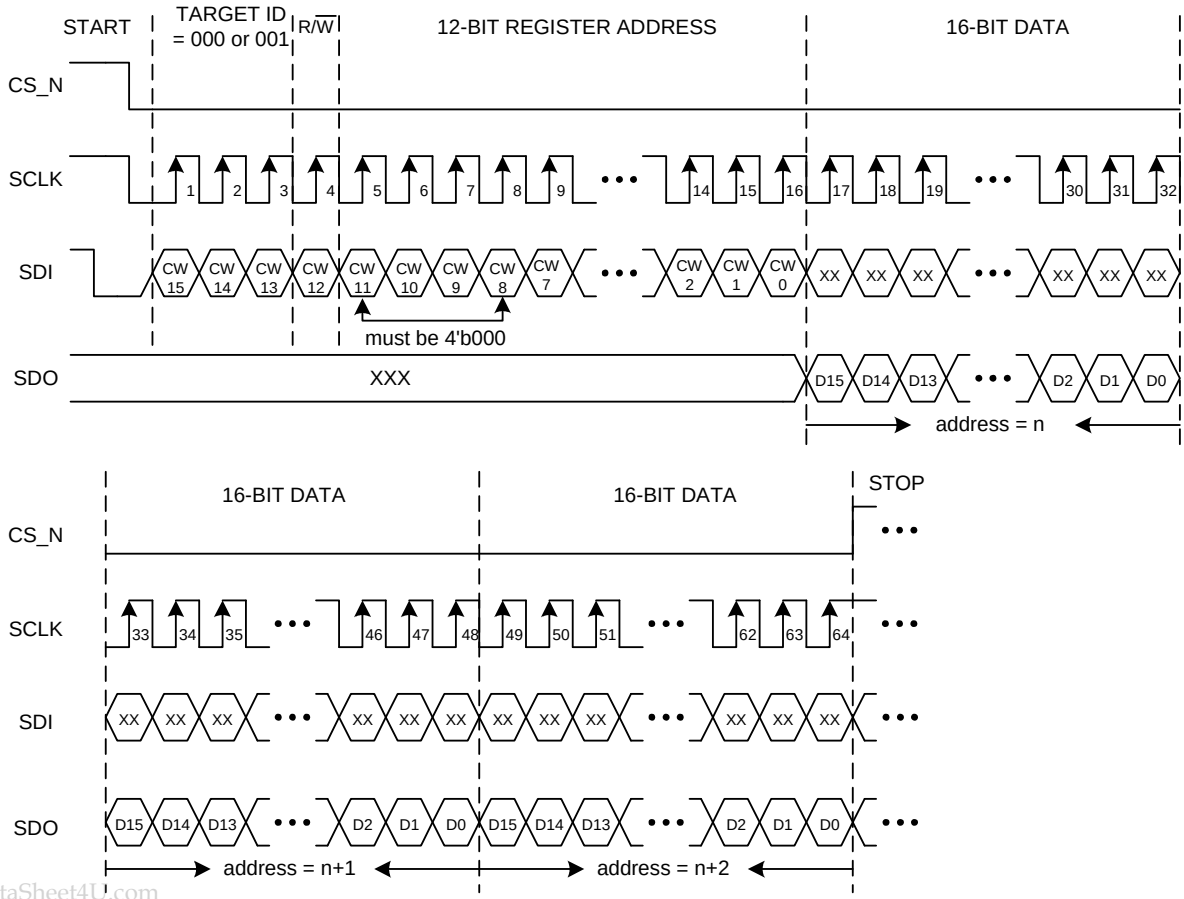


Figure 7-6. Example of SPI Timing for Burst Register Read Operation



8. DC Characteristics

Absolute Maximum Ratings

Power Supply (DVCC) ..... -0.3V to 3.6V

Power Supply (AVCC) ..... -0.3V to 3.6V

Input Voltage ..... -0.3V to DVCC + 0.3V

Output Voltage ..... -0.3V to DVCC + 0.3V

Storage Temperature ..... -40°C to 125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Operation Condition Vcc=3.0V~3.6V, Tj=0°C~115°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	CMOS	-	-	0.3*DVCC	V
V_{IH}	Input High Voltage	CMOS	0.7*DVCC	-	-	V
Vt-	Schmitt trigger negative going threshold voltage	CMOS	-	1.80	-	V
Vt+	Schmitt trigger positive going threshold voltage	CMOS	-	2.10	-	V
V_{OL}	Output Low Voltage	I_{OL}=2mA	-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}=2mA	2.4	-	-	V
R_I	Input Pull-up Resistance	V_{IL}=0V or V_{IH}=DVCC	-	75	-	KΩ
I_{IL}	Input Leakage Current	no pull-up	-1	-	1	uA
I_{OZ}	Tri-state Leakage Current		-1	-	1	mA
C_{IN}	Input Capacity		-	10	-	pF
C_{OUT}	Output Capacity		-	10	-	pF
C_{BID}	Bi-directional Buffer Capacity		-	10	-	pF

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9. AC Characteristics

Figure 9-1. Definition of Timing for I²C Interface

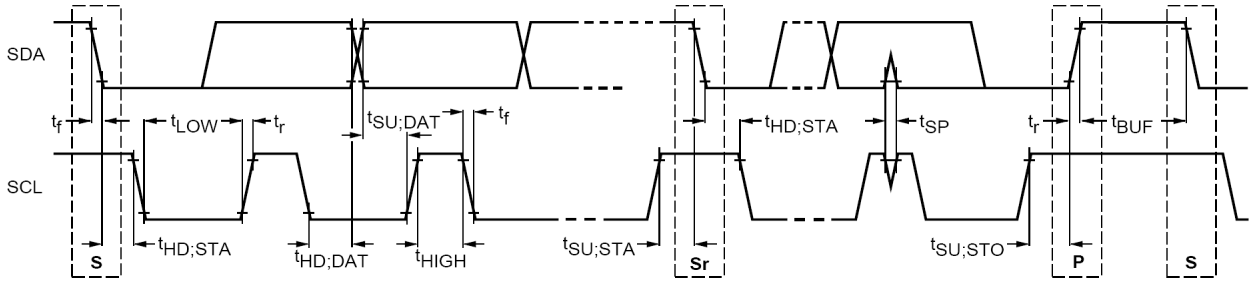


Table 9-1. I²C AC Characteristic

Symbol	Parameter	Min.	Max.	Unit
f_{SCL}	SCL clock frequency	1	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6	-	us
t_{LOW}	LOW period of the SCL clock	1.3	-	us
t_{HIGH}	HIGH period of the SCL clock	0.6	-	us
$t_{SU;STA}$	Set-up time for a repeated START condition	0.6	-	us
$t_{HD;DAT}$	Data hold time	0	0.9	us
$t_{SU;DAT}$	Data set-up time	100	-	ns
t_r	Rise time of both SDA and SCL signals	$20+0.1C_b$	300	ns
t_f	Fall time of both SDA and SCL signals	$20+0.1C_b$	300	ns
$t_{SU;STO}$	Set-up time for STOP condition	0.6	-	us
t_{BUF}	Bus free time between a STOP and START condition	1.3	-	us
C_b	Capacitive load for each bus line	-	400	pF
V_{nL}	Noise margin at the LOW level for each connected device (including hysteresis)	$0.1V_{DD}$	-	V
V_{nH}	Noise margin at the HIGH level for each connected device (including hysteresis)	$0.2V_{DD}$	-	V
$t_{timeout}$	Cumulative SCL low timeout limit	3	5	ms

Figure 9-2. Definition of Timing for SPI Interface

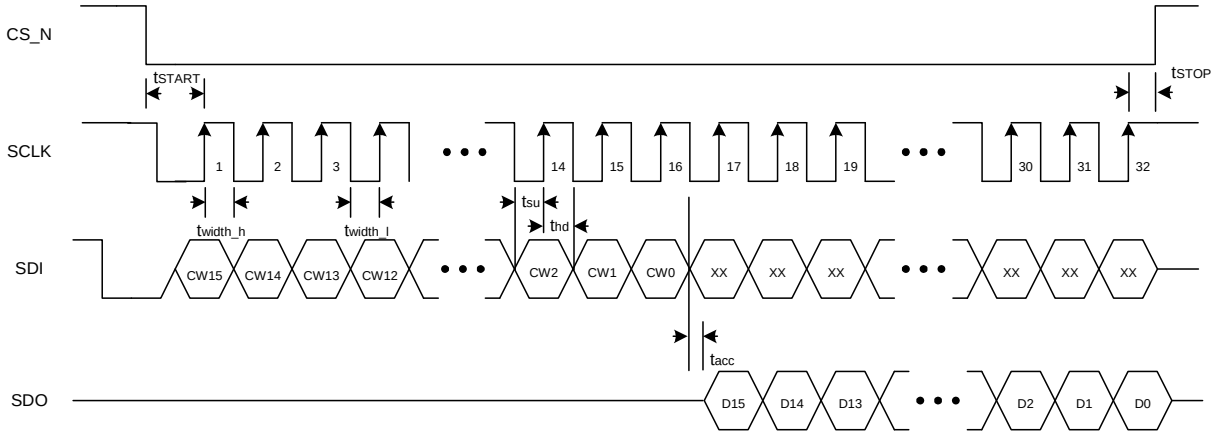
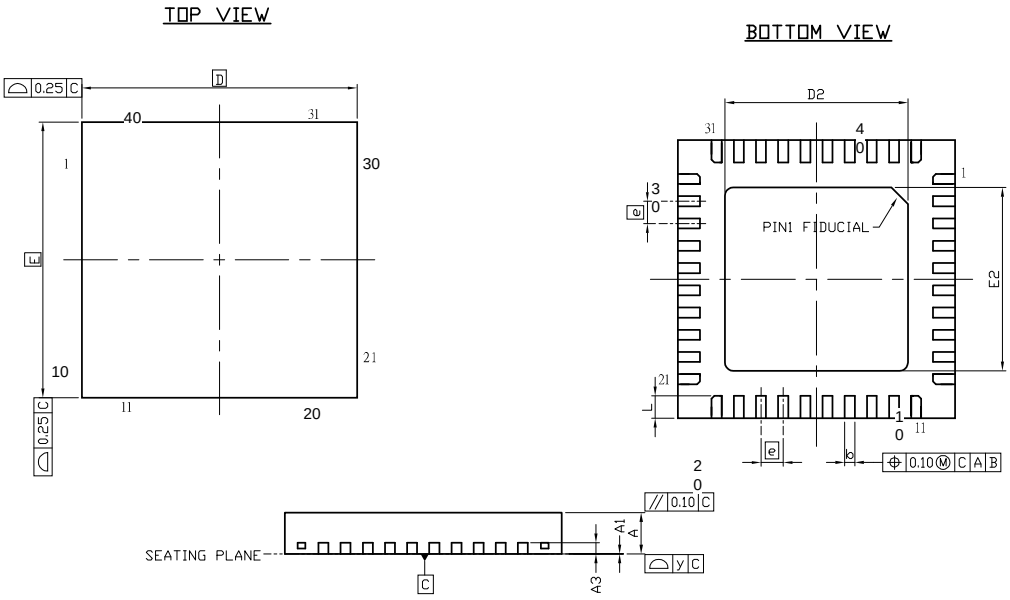


Table 9-2. SPI AC Characteristic

Symbol	Parameter	Min.	Max.	Unit
f_{SCLK}	SCKL clock frequency	0	5	MHz
t_{START}	CS_N falling to SCLK rising edge	10	-	ns
t_{STOP}	SCLK rising to CS_N rising edge	10	-	ns
t_{width_h}	SCLK high pulse width	20	-	ns
t_{width_l}	SCLK low pulse width	20	-	ns
t_{SU}	SDI to SCLK Setup time	10	-	ns
t_{HD}	SDI to SCLK hold time	10	-	ns
t_{acc}	SDO access time after SCLK falling edge	-	20	ns

10. Package Information

QFN 40L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.028	0.030	0.032	0.70	0.75	0.80
A_1	0.000	0.0008	0.002	0.00	0.02	0.05
A_3	0.008 REF			0.203 REF		
b	0.006	0.008	0.010	0.15	0.20	0.25
D	0.197BSC			5.00 BSC		
D2	0.126	0.130	0.134	3.20	3.30	3.40
E	0.197BSC			5.00BSC		
E2	0.126	0.130	0.134	3.20	3.30	3.40
e	0.016 BSC			0.40 BSC		
L	0.012	0.014	0.016	0.35	0.40	0.45
y	--	--	0.003	--	--	0.08

Notes:

1. CONTROLLING DIMENSION：MILLIMETER
2. REFERENCE DOCUMENT：JEDEC MO-220.

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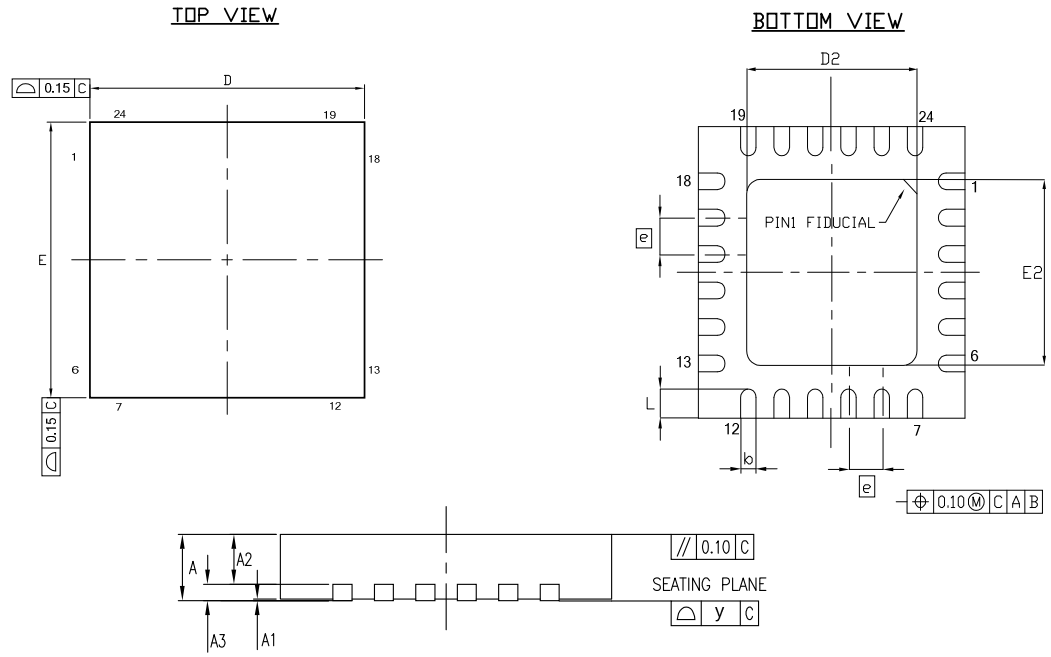
QFN 24L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.030	0.031	0.033	0.76	0.80	0.84
A1	0.000	0.0008	0.0015	0.00	0.02	0.04
A2	0.022	0.024	0.025	0.57	0.60	0.63
A3	0.008 REF			0.20 REF		
b	0.007	0.010	0.012	0.18	0.25	0.30
D	0.157 BSC			4.00 BSC		
D2	0.098	0.100	0.102	2.50	2.55	2.60
E	0.157 BSC			4.00 BSC		
E2	0.098	0.100	0.102	2.50	2.55	2.60
e	0.020 BSC			0.50 BSC		
L	0.012	0.014	0.016	0.35	0.40	0.45
y	--	--	0.003	--	--	0.08

Notes:

1. CONTROLLING DIMENSION：MILLIMETER
2. REFERENCE DOCUMENT：JEDEC MO-220.

DI-QFN24(4*4)v0

11. Ordering Information

Part No.	Package	Code No.
IT7230AFN	QFN40	CCCC
IT7230BFN	QFN24	CCCC
IT7231FN	QFN40	CCCC

Code No.: 0000 ~ FFFF

Example:

1. IT7230AFN/BX—0001
2. IT7230BFN/BX—0005
3. IT7231FN/CX—0007
4. .....

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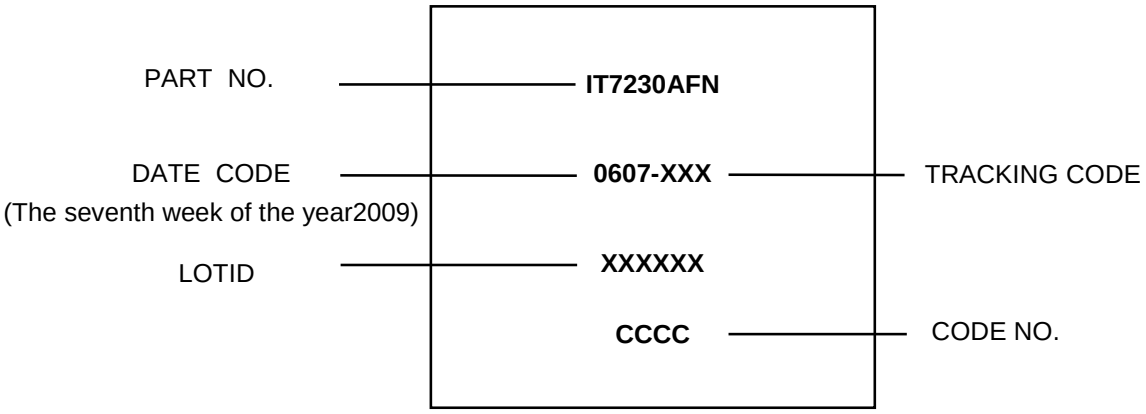
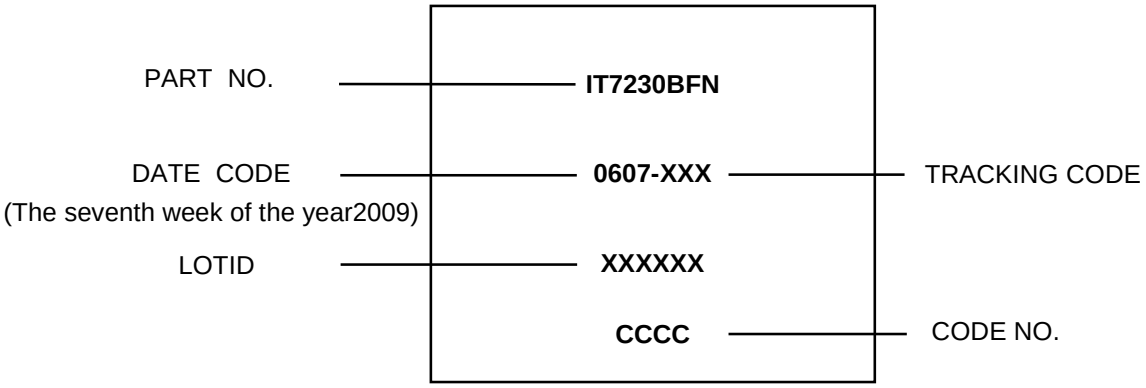
12. Top Marking Information

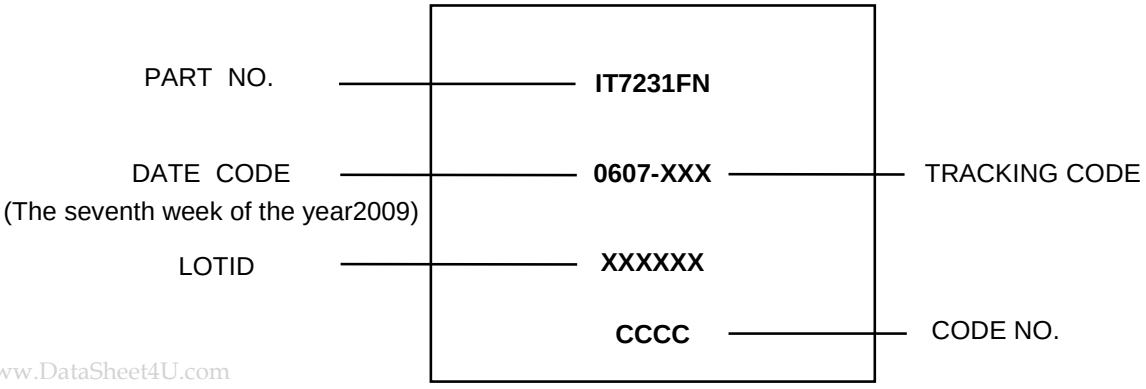
a. IT7230AFN (QFN40)



b. IT7230BFN (QFN24)



c. IT7231FN (QFN40)



ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2005)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc..

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.
(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.
(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.
(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.
(b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.
(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.
(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.
(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.
(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.
(c) Buyer will not return any goods without first obtaining a customer return order number.
(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.
(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.
(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.
Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement.
Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.
(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.